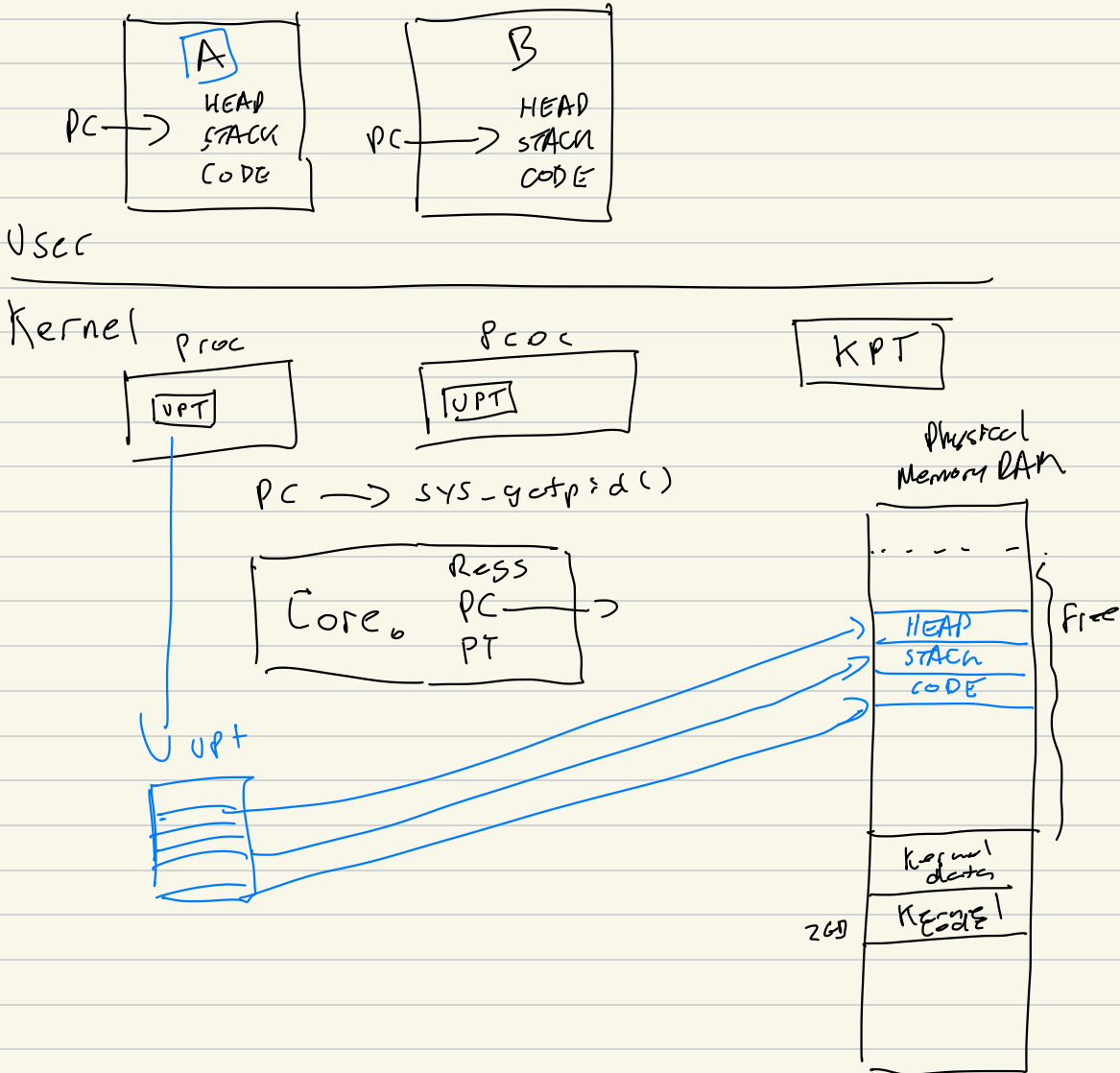


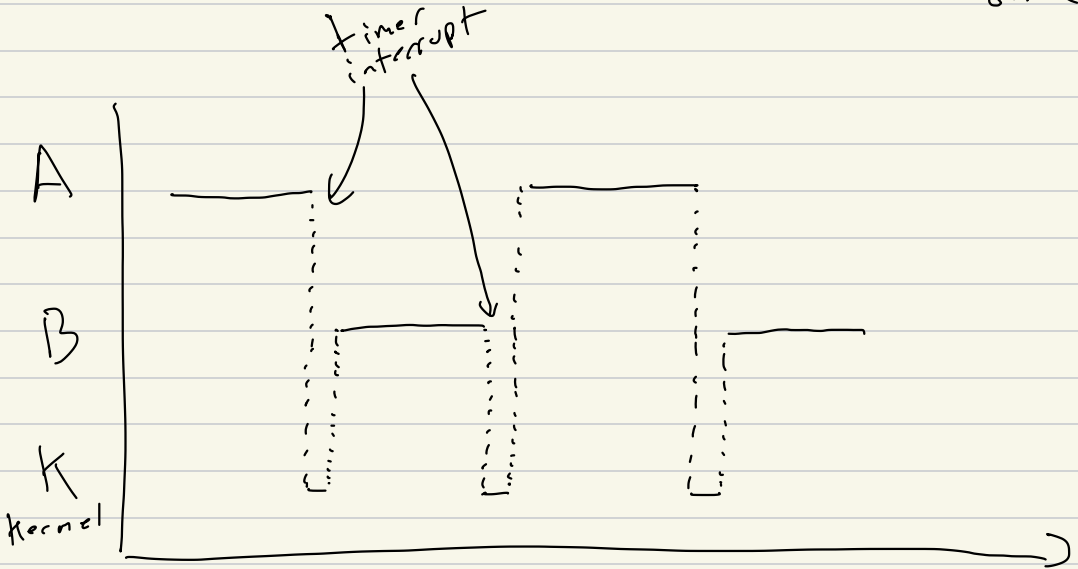
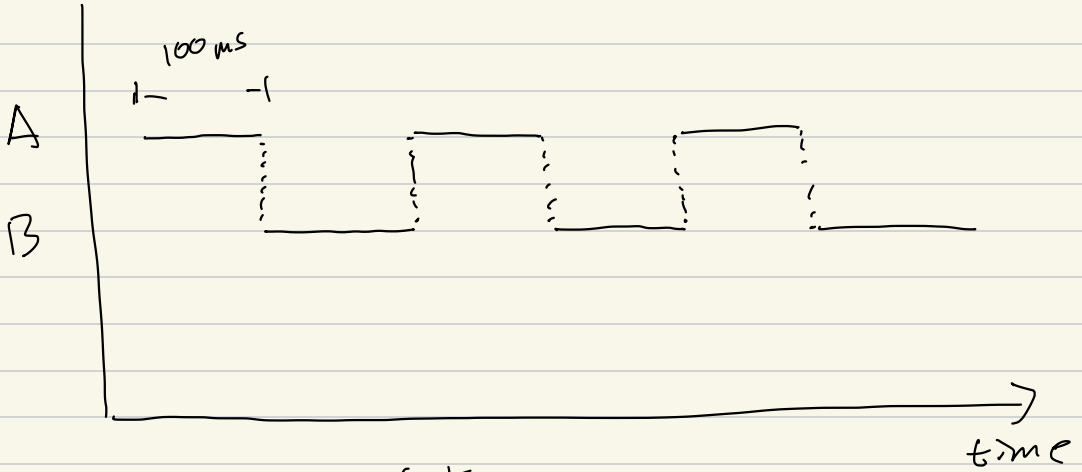
Process scheduling
Page Tables

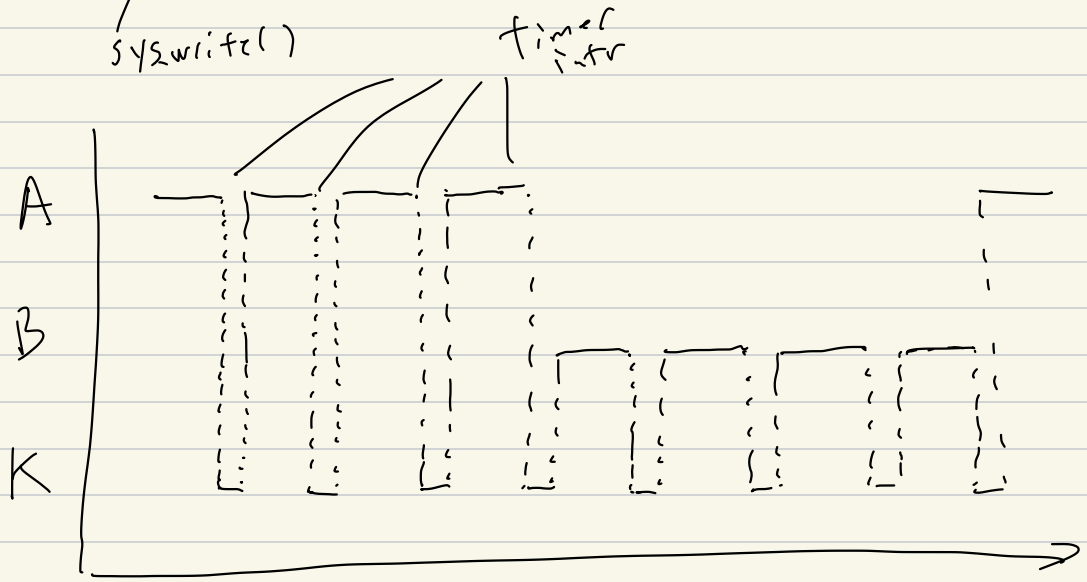
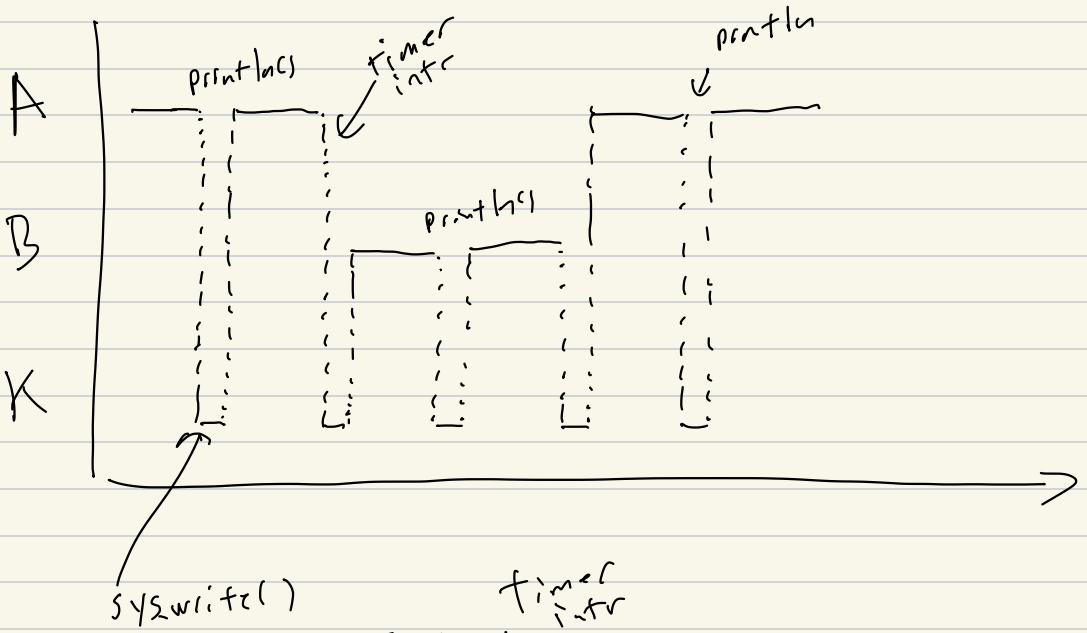


(A)

(B)

CORE

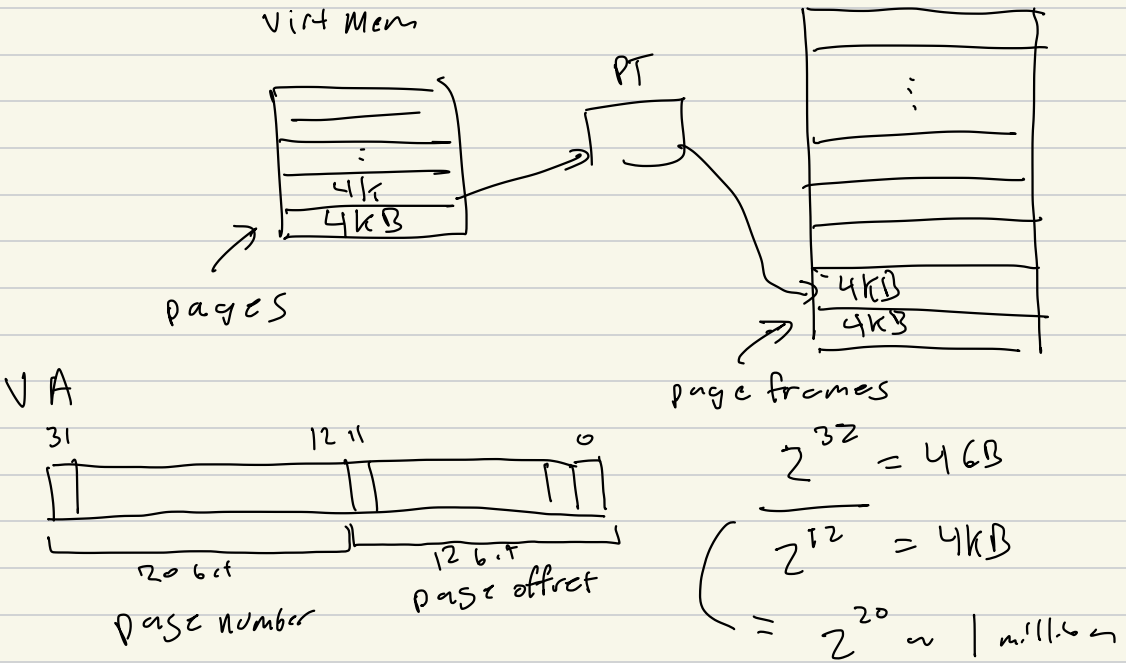




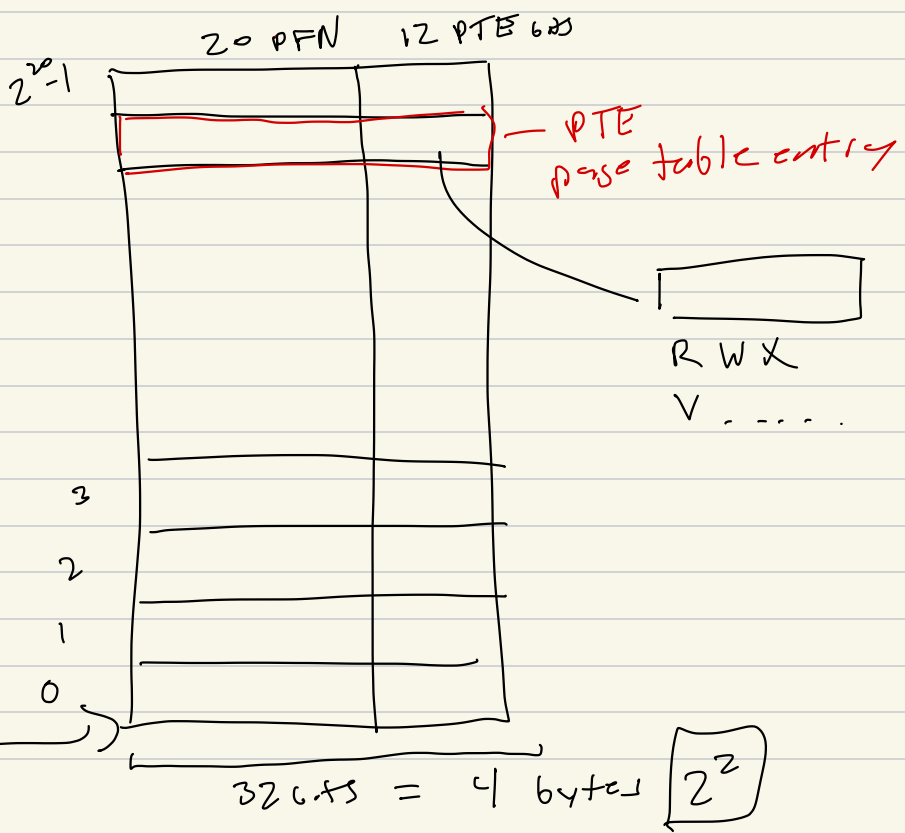
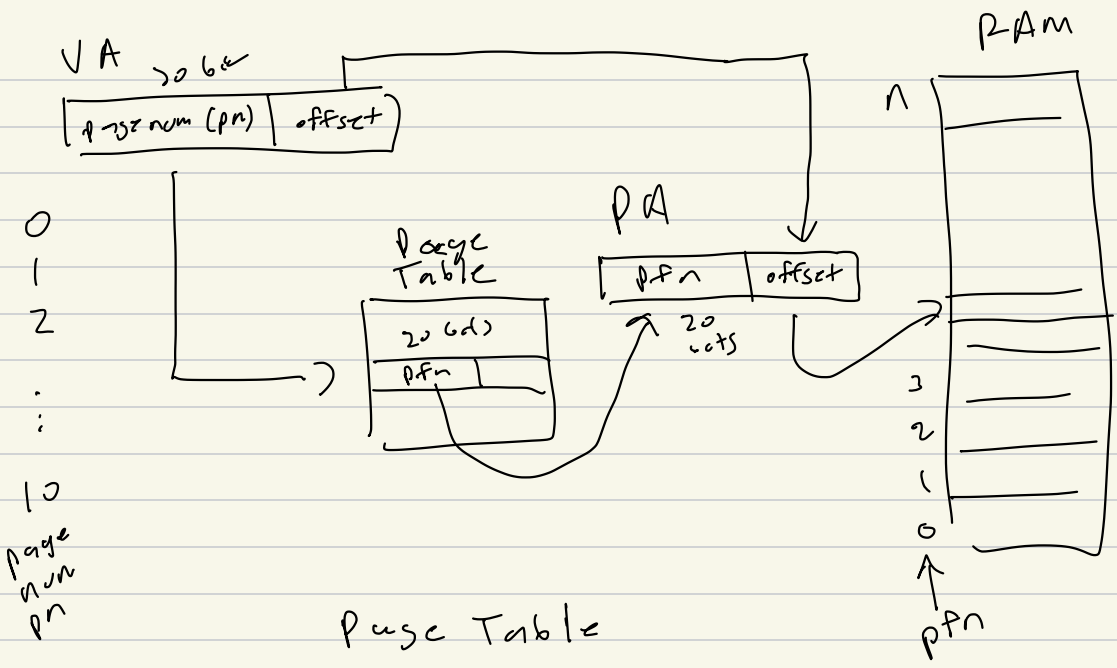
Page Tables (Virtual Memory)

Assume a 32 bit architecture $2^{32} = 4GB$

Physical Address (PA) Page size (4KB)
 Virtual Address (VA) Phys Mem $2^{12} = 4KB$



VA \rightarrow PA

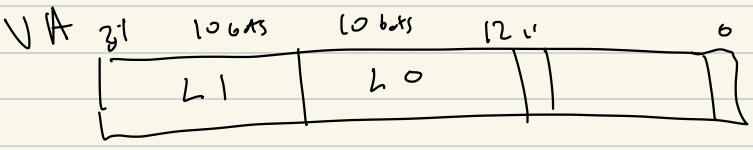


Size of the page table

$$2^2 \times 2^{20} = 2^{22} = \boxed{4 \text{ MB}}$$

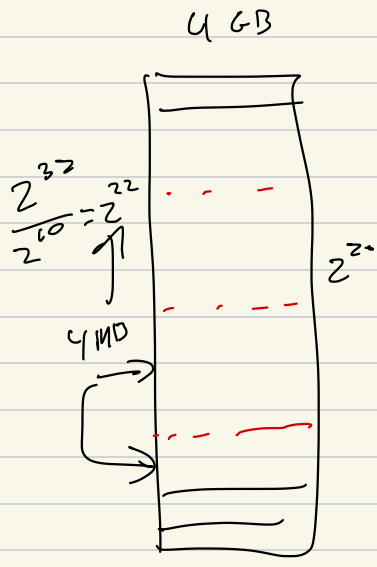
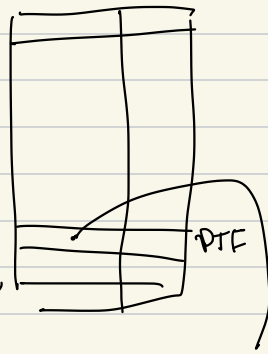
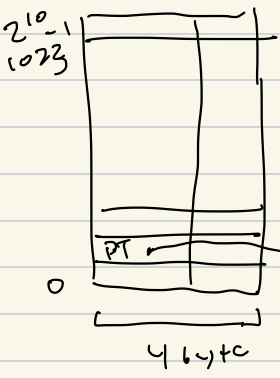
100 procs $100 \times 4 = \boxed{400 \text{ MB}}$

Multi-level Page Tables (Sparse)



L1 Page Table

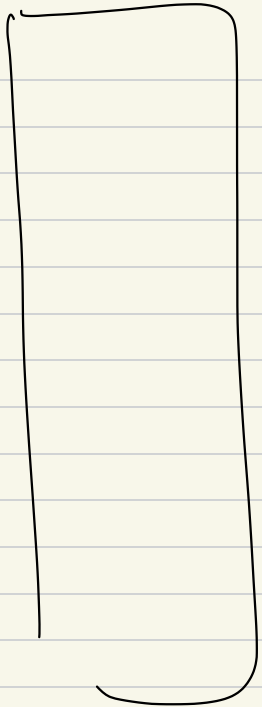
L0 Page



$$2^{10} \times 2^2 = 2^{12} = 4 \text{ KB}$$

PFN

Phys RAM

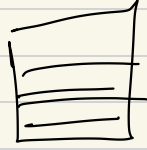


Cache

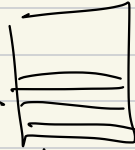
L1



L2 4KB



L2 4KB



L2 4KB

